

Description

HIGH POWER SPACE TRANSFORMER

BACKGROUND OF INVENTION

[0001] FIELD OF THE INVENTION

[0002] The present invention relates to the field of integrated circuit chip testing; more specifically, it relates to a space transformer for use in a system for testing integrated circuit chips on a wafer.

[0003] BACKGROUND OF THE INVENTION

[0004] Typical wafer level test of integrated circuit chips consists of a set of probes for contacting controlled collapse chip connections (C4s also known as solder bumps) and contact pads of the integrated circuit chip mounted to a space transformer which in turn is mounted to a probe card, the probe card is in turn connected to a tester. The tester supplies power, ground and signals to the integrated circuit chip also known as a device under test (DUT). Three basic problems must be overcome when testing semiconductor integrated circuit chips in this manner. First, the amount of power to be supplied must be sufficient to respond to power surges while transistors and other devices in the integrated circuit chip are switching. Second, as power surges occur, coupling noise on signal lines is generated which must be minimized. Third, with high power consumption integrated circuits unwanted heat generation within the space transformer can occur.

SUMMARY OF INVENTION

[0005] A first aspect of the present invention is a space transformer comprising: a ground conductor; a power conductor; and one or more decoupling capacitors physically located between the ground conductor and the power conductor and electrically connected between a bottom surface of the ground conductor and a top surface of the power conductor.

[0006] A second aspect of the present invention is a wafer test apparatus comprising: a probe card; a space transformer mounted to the probe card, the space transformer comprising: a ground conductor; a power conductor; and one or more decoupling capacitors physically located between the ground conductor and the power conductor and electrically connected between a bottom surface of the ground conductor and a top surface of the power conductor; and a probe mounted to the space transformer.

[0007] A third aspect of the present invention is a space transformer comprising: a ground conductor; a power conductor; one or more additional conductors; one or more decoupling capacitors physically located between the ground conductor and the power conductor and electrically connected between the ground conductor the power conductor and between the ground conductor and the additional conductors; one or more ground pins fixed to and extending from the ground conductor to a top surface of a product die mounted on a top surface of the ground conductor; one or more power pins fixed to and extending from the power conductor to the top surface of the product die; one or more additional pins fixed to and extending from the additional conductor to the top surface of the product die; and one or more

signal wires extending from a bottom surface of a board die mounted to a bottom surface of the power conductor to the top surface of the space transformer.

BRIEF DESCRIPTION OF DRAWINGS

[0008] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein: FIG. 1A is a top view and FIG. 1B is a cross-sectional view through line 1B-1B of FIG. 1A of a first element of a space transformer according to the present invention; FIG. 2A is a top view and FIG. 2B is a cross-sectional view through line 2B-2B of FIG. 2A of a second element of the space transformer according to the present invention; FIG. 3A is a top view and FIG. 3B is a cross-sectional view through line 3B-3B of FIG. 3A of a third element of the space transformer according to the present invention; FIG. 4A is a top view and FIG. 4B is a cross-sectional view through line 4B-4B of FIG. 4A of a fourth element of the space transformer according to the present invention; FIG. 5A is a top view and FIG. 5B is a cross-sectional view through line 5B-5B of FIG. 5A of a first element of the space transformer according to the present invention; FIG. 6A is a top view and FIG. 6B is a cross-sectional view through line 6B-6B of FIG. 6A of a first element of the space transformer according to the present invention FIG. 7A is cross-sectional view of an assembled space transformer according to the present invention; FIG. 7B is an enlarged cross-sectional view of a portion of the assembled space transformer of FIG. 7A; FIG. 8 is a side view of a typical ground or power pin

according to the present invention; FIG. 9A is cross-sectional view and FIG. 9B is a side view of a probe assembly according to the present invention, FIG. 10 is a partial cross-sectional view of a thin film interface (TFI) probe; FIG. 11 is a partial side view of an integrated circuit chip wafer under test; FIG. 12A is cross-sectional view of an assembled space transformer according to a second embodiment of the present invention; FIG. 12B is cross-sectional view of an assembled space transformer according to a third embodiment of the present invention; and FIG. 13 is a cross-sectional view of an assembled space transformer according to a fourth embodiment of the present invention.

DETAILED DESCRIPTION

[0009] The goal of a "good" power delivery system, and this critically includes the space transformer portion of that system, is to provide the device under test (DUT), an integrated circuit chip, with minimal power supply voltage variations throughout the dynamic operating range of the DUT and to minimize inductance and resistance between the power supply and the DUT while at the same time providing sufficient local power storage to supply instantaneous demands of high speed transistor switching. The power delivery system results in an inductance-resistance-capacitance (LRC) network with complex transfer characteristics that vary over a wide signal frequency spectrum. A "good" power delivery system will minimize the inductance and resistance while providing capacitive decoupling.

[0010] At low signal frequencies (DC to KHz) the large decoupling capacitors (thousands of μF) are utilized. At mid signal frequencies (KHz to hundreds of

MHz) relatively small (tens of μF) decoupling capacitors are used. At high signal frequencies (GHz and up) very small (sub μF) decoupling capacitors that are also very low inductance capacitors (1 nano Henry to 10 pico Henries) are used. While the total inductance between the decoupling capacitor and the DUT must be minimized (and this includes capacitor parasitic, interconnection and probe inductance) for mid signal frequency devices it is especially important to do so for high signal frequencies. The present invention solves these problems by providing a robust ground and power network and by placing the decoupling capacitors very close to the test probes.

[0011] A "space transformer" is so called because it transforms the spacing of chip contacts with respect to an integrated circuit chip to a larger spacing that will accommodate printed circuit board (PCB) wiring and/or conventional wires. A chip contact is defined as a C4, solder bump, contact pad, non-solder bump or other electrical chip connection known in the art. The space transformer of the present invention includes six elements that will be illustrated and described in turn.

[0012] FIG. 1A is a top view and FIG. 1B is a cross-sectional view through line 1B-1B of FIG. 1A of a first element of the space transformer according to the present invention. In FIGs. 1A and 1B, a product die 100 includes a multiplicity of through-holes 105 arranged in the same pattern and to the same pitch (chip contact to chip contact distance) as the chip contacts on an integrated circuit chip to be tested. While an exemplary 5 by 5 array of through-holes 105 is illustrated in FIG. 1A, it should be understood that there may be thousands of chip contacts arranged in any number of patterns on

an integrated circuit chip. In one example, through-holes 105 have a diameter D1 of about 0.0055 inches when un-insulated wires and pins are used and about 0.0065 when insulated wires and pins are used, and product die 100 has a thickness T1 of about 0.030 inches. Product die 100 is fabricated from a dielectric material. In one example product die 100 is fabricated from VespelTM (a polyimide resin), manufactured by Dupont, Wilmington, DE.

[0013] FIG. 2A is a top view and FIG. 2B is a cross-sectional view through line 2B-2B of FIG. 2A of a second element of the space transformer according to the present invention. In FIGs. 2A and 2B a ground conductor 110 includes a multiplicity of through-holes 115 arranged in the same pattern and to the same pitch as through-holes 105 of FIG. 1A. Ground conductor 110 includes an inner region 120, which includes through-holes 115, and an outer region 125. In one example, through-holes 115 have a diameter D1 of about 0.0055 inches and inner region 120 of ground conductor 110 has a thickness T2 of about 0.030 inches. Ground conductor 110 is fabricated from a conductive material. In one example, ground conductor 110 is fabricated from a metal such as copper or aluminum. Ground conductor 110 is (conventionally) electrically connected to a ground terminal of a power supply.

[0014] FIG. 3A is a top view and FIG. 3B is a cross-sectional view through line 3B-3B of FIG. 3A of a third element of the space transformer according to the present invention. In FIGs. 3A and 3B, a capacitor board 130 includes a ring 135 surrounding an opening 140 and decoupling capacitors 145 mounted on an underside 150 of ring 135. In one example, capacitor board 130 has a thickness T3 of about 0.012 inches. Capacitor board 100 is

abricated from a dielectric material. In one example, product die 130 is a PCB and includes wiring traces (not shown) suitable for mounting decoupling capacitors 145 and interconnecting the decoupling capacitors between ground conductor 110 (see FIGs. 4A, 4B and 7) and a power conductor 155 (see FIGs. 4A, 4B and 7). While only 20 decoupling capacitors are illustrated in FIGs. 3A and 3B, the number of decoupling capacitors is limited only by physical space constraints and can range up to a hundred or more based on a design that provides the best decoupling. In a first example, decoupling capacitors 145 are low inductance decoupling capacitor arrays (LICA) developed by IBM, Armonk, NY and AVX, Myrtle Beach, CA. In a second example, decoupling capacitors 145 are multilayer ceramic capacitors such as 1210 series capacitors. In a third example, decoupling capacitors 145 are IBM proprietary C4 capacitors. In one example, decoupling capacitors 145 can have inductance values ranging from about 1 nano-Henry to about 175 pico-Henries and in a second example for high frequency application, decoupling capacitors 145 can have inductance values of 60 pico-Henries or less.

[0015] FIG. 4A is a top view and FIG. 4B is a cross-sectional view through line 4B-4B of FIG. 4A of a fourth element of the space transformer according to the present invention. In FIGs. 4A and 4B power conductor 155 includes a multiplicity of through-holes 160 arranged in the same pattern and to the same pitch as through-holes 105 of FIG. 1A with the exception that there is no through-hole 160 in any position corresponding to a chip contact of the integrated circuit chip that carries ground. Power conductor 155 includes an inner region 165, which includes through-holes 160, and an outer region 170 that includes recesses 170 for receiving decoupling capacitors 145 (see

FIGs. 3A and 3B). In one example, through-holes 160 have a diameter D1 and inner region 165 of power conductor 155 has a thickness T4 of about 0.030 inches. Power conductor 155 is fabricated from a conductive material. In one example, power conductor 155 is fabricated from a metal such as copper or aluminum. Note no through holes 160 are formed in power conductor 155 in chip contact position that will be connected to ground. Power conductor 155 is (conventionally) electrically connected to a power terminal of the power supply.

[0016] FIG. 5A is a top view and FIG. 5B is a cross-sectional view through line 5B-5B of FIG. 5A of a first element of the space transformer according to the present invention. In FIGs. 5A and 5B, an inner die 180 includes a multiplicity of through-holes 185 arranged in the same pattern and to the same pitch as through-holes 105 of FIG. 1A except there is no through-hole 185 in any position corresponding to a chip contact of the integrated circuit chip that carries ground or power. In one example, through-holes 185 have a diameter D1 and inner die 180 has a thickness T5 of about 0.015 inches. Inner die 180 is fabricated from a dielectric material. In one example, inner die 180 is fabricated from VespelTM. Note no through holes 185 are formed in inner die 180 in chip contact position that will be connected to ground or power.

[0017] FIG. 6A is a top view and FIG. 6B is a cross-sectional view through line 6B-6B of FIG. 6A of a first element of the space transformer according to the present invention. In FIGs. 6A and 6B, a board die 190 includes a multiplicity of through-holes 195 arranged in a pattern corresponding to the pattern of through-holes 105 of FIG. 1A except there is no through-hole 195 in any

sition corresponding to a chip contact of the integrated circuit chip that carries ground or power or is unused and except that the pitch between through-holes 195 is significantly greater than the pitch between through-holes 105 . In one example, through-holes 195 have a diameter D2 and board die 190 has a thickness T6 of about 0.020 inches. Board die 190 is fabricated from a dielectric material. In one example, board die 190 is fabricated from VespelTM.

[0018] FIG. 7A is cross-sectional view of an assembled space transformer according to the present invention. In FIG. 7A, assembled space transformer 200, product die 100, top ground conductor 110, capacitor board 140 (including decoupling capacitors 145), power conductor 155, inner die 180 and board die 190. Assembly fasteners and alignment pins and holes have been omitted for clarity. Product die 100 is mounted on a top surface 110A of ground conductor 110. Capacitor board 140 is mounted between and in contact with a bottom surface 110B of ground conductor 110 and a top surface 155A of power conductor 155. In the present example, decoupling capacitors 145 are surface mounted (either C4 or SMT) to capacitor board 140 and conductive wires (not shown) in the capacitor board connect a first plate of each decoupling capacitor to ground conductor 110 and a second plate of each decoupling capacitor to power conductor 155. Inner die 180 is mounted to a bottom surface 155B of inner region 165 of power conductor 155 and board die 190 is mounted in notches formed in a bottom surface 155C of outer region 170 of the power conductor. Electrically conductive ground pin 205, power pin 215 and signal wires 215 are described infra with respect to FIG. 7B. A space 225 between inner die 180 and board die 190 is filled with a dielectric material 220. The space between bottom surface 110A

of ground conductor 110 and top surface 155A of power conductor 155 is filled with dielectric material 220.

[0019] It should be noted that decoupling capacitors 145 are physically located between power conductor 155 and ground conductor 110 reducing to minimum the capacitor interconnect inductance and resistance parasitics. The length of the electrical path between decoupling capacitors 145 and tips of ground pins 205 and power pins 210 at the surface of space transformer 200 is between about 5 to 25 millimeters. The length of the electrical path between the tips of ground pins 205 and power pins 210 at the top surface of space transformer and ground conductor 110 and power conductor 155 respectively is about 1 to 3mm. Also, because of the thickness of inner regions 120 of ground conductor 110 and inner region 165 of power conductor 155, resistive parasitics are reduced and more current can be carried with reduced voltage drop. Because of the location of decoupling capacitors 145 within space transformer 200, more decoupling capacitance is available than with conventional space transformers.

[0020] While one power conductor and one ground conductor are illustrated in FIG. 7A, it is possible for one of ordinary skill in the art to extend the present invention to include a space transformer having more than one power conductor and/or more than one ground conductor stacked in ground/power conductor pairs. Decoupling capacitors could be included between each ground/power conductor pair.

[0021] FIG. 7B is an enlarged cross-sectional view of a portion of the assembled space transformer of FIG. 7A. In FIG. 7B it may be seen that through-holes

105 in product die 100 , through-holes 115 in ground conductor 110, through-holes 160 in power conductor 155 and through-holes 185 in inner die 180 are co-aligned. Ground pin 205 is fixed to ground conductor 115 by being pressed (swaged) into through-hole 115 in ground conductor 110 and passes through through-hole 105 in product die 100. Power pin 210 is fixed to power conductor by being pressed (swaged) into through-hole 160 in power conductor 155 and passes through through-hole 115 in ground conductor 110 and through-hole 105 in product die 100. Instead of pressing power and ground pins into their respective conductors, other means to form physical and electric contact between pins and conductors, such as soldering, may be used. Signal wires 215 are fixed in through-holes 195 in board die 190 by dielectric material 220 . Signal wires 215 pass through through-holes 185 in inner die 180, through-holes 160 in power conductor 155, through-holes 115 in ground conductor 110 and through-holes 105 in product die 100. Ground pin 205, power pin 210 and signal wires 215 have diameters less than the diameter of through-holes 105, 115, 160 and 185. Ground pins 205, power pins 215 and signal wires 215 are illustrated as un-insulated. Insulated ground pins and/or insulated power pins and/or insulated signal wires or combinations of insulated and un-insulated wires and pins may be used.

[0022] FIG. 8 is a side view of a typical ground or power pin according to the present invention. In FIG. 8, ground/power pin 205/210 has an upper region 230 having a diameter of D_4 and a bottom region (swage region) having a diameter of D_5 . In one example, when D_1 (see, for example, FIG. 1A) is about 0.0055 inches, D_3 is about 0.005 inches and D_4 is about 0.006 inches.

[0023] FIG. 9A is cross-sectional view and FIG. 9B is a side view of a probe assembly 250 according to the present invention. In FIGs. 9A and 9B, probe assembly 250 includes a probe card 255, an interposer 260, space transformer 200 and a probe 265. Probe 265 includes an array of probe tips 270 having the same pattern and pitch as the chip contact connectors on a DUT. Probe card 255 includes a multiplicity of interconnects 275 electrically connected to probe tips 270 through interposer 260 and space transformer 200. Interposer 260 interconnects ground conductor 110 (see FIGs. 7A and 7B), power conductor 155 (see FIGs. 7A and 7B) and signal wires 215 (see FIGs. 7A and 7B) to interconnects 275 on probe card 255. A portion of interconnects 275 on probe card 255 are connected to ground conductor 110 (see FIGs. 7A and 7B) and power conductor 155 (see FIGs. 7A and 7B) of space transformer 200 (see FIGs. 7A and 7B). Interconnects 275 are also connected to wires that go to a tester (not shown). Interposer 260 is mounted to a top surface 255A of probe card 255. Space transformer 200 is mounted to a top surface 260A of interposer 260. Probe 265 is mounted to top surface 110A of ground conductor 110 (see FIGs. 7A and 7B) of space transformer 200 (see FIGs. 7A and 7B). Probe tips 270 electrically contact ground pins 205, power pins 210 and signal wires 215 of space transformer 200. Assembly fasteners and alignment pins and holes have been omitted for clarity.

[0024] FIG. 10 is a partial cross-sectional view of probe 265. Probe 265 is a thin film interface (TFI) probe. Probe tips 270 interlock in holes 275 in dielectric membrane 280. Other types of probes, for example cantilevered probes (probes where the probes tips extend over the DUT from a support), spring-loaded probes, i. e. COBRA probes, (where an array of spring-loaded

contacts is placed over the DUT) and other types of probes equally well known in the art may also be used, but TFI probes have less parasitics and reduce the power, ground and signal electrical path lengths.

[0025] FIG. 11 is a partial side view of an integrated circuit chip wafer 285 under test. In FIG. 11, an integrated circuit chip wafer 285 is held on a stepping stage 290 free to move in two orthogonal co-planer directions as well as rotate about an axis perpendicular to the co-planer directions. Wafer 285 includes an array of chip contact interconnect 295 corresponding to multiple chips on the wafer. Probe tips 270 contact chip contact interconnects 295 and ground pins 205, power pins 210, and signal wires 215 of space transformer 200 when probe assembly 250 and wafer 285 are brought together. Stage 290 allows stepping from one chip to another in order to test all chips on the wafer.

[0026] FIG. 12A is a cross-sectional view of an assembled space transformer according to a second embodiment of the present invention. In FIG. 12A, space transformer 200A differs from space transformer 200 of FIG. 7A, only in the fact that outer region 125 of ground conductor 110 includes a channel 295 whereby a cooling or heating fluid (liquid or gas) may be circulated to cool or heat not only the space transformer but also the DUT by heat flow through the chip contact interconnects of the DUT.

[0027] FIG. 12B is a cross-sectional view of an assembled space transformer 200B according to a third embodiment of the present invention. In FIG. 12A, space transformer 200B differs from space transformer 200 of FIG. 7A, only in the fact that outer region 170 of power conductor 155 includes a channel 300

hereby a cooling or heating fluid (liquid or gas) may be circulated to cool or heat not only the space transformer but also the DUT by heat flow through the chip contact interconnects of the DUT.

[0028] A fourth embodiment of the present invention would include both channel 295 (see FIG. 12A) in outer region 125 of ground conductor 110 and channel 300 (see FIG. 12B) in outer region 170 of power conductor 155.

[0029] FIG. 13 is a cross-sectional view of an assembled space transformer according to a fourth embodiment of the present invention. In FIG. 13, an additional conductor 305 (which may be electrically connected to power or ground) is positioned between power conductor 155 and inner die 180. Additional conductor 305 electrically contacts capacitor board 140 via extensions 310 passing through through-holes 315 in power conductor 155. A space 320 between power conductor 170 and additional conductor 305 is filled with dielectric material 220. More additional conductors may be added as required in a similar manner as additional conductor 305.

[0030] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. For example, instead of the ground conductor being electrically connected to the ground terminal of a power supply, ground conductor may be electrically connected to the power terminal of the power supply and instead of the power conductor being electrically connected to

the power terminal of the power supply, the power conductor may be electrically connected to the ground terminal of the power supply. The present invention was described with the outermost conductor being electrically connected to the ground terminal of the power supply for safety and to comply with equipment design conventions. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.